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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,013	11/26/2001	James E. Jaussi	884.512US1	9548

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,013	JAUSSI ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-20* is/are allowed.

6)☒ Claim(s) *1-5,7-9,21 and 27* is/are rejected.

7)☒ Claim(s) *6, 22-26, 28-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 is indefinite because there is no means that perform the function of "copy the generated current".

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1 and 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Wada et al. (US 2002/0036536 A1).

As to claim 1, Wada et al discloses in figure 2 a current reference comprising: a current mirror circuit (11, 12) to force a first current to be substantially equal to a second current; a control transistor (13) coupled to the current mirror circuit to receive the first current, the control

transistor having first and second biasing terminals (gate and source) across which a biasing voltage can be applied; and a variable resistor (R1) coupled between the first and second biasing terminals of the control transistor and coupled to the current mirror to receive the second current.

As to claim 7, figure 2 shows the control transistor (13) comprises a NFET, and the first and second biasing terminals are a gate source of the NFET.

As to claim 8, figure 2 shows a second NFET (14) having a drain terminal coupled to receive the second current from the current mirror, and having a source terminal coupled to provide the second current to the variable resistor.

As to claim 9, figure 2 shows a transistor (14) coupled drain-to-source between the current mirror and the variable resistor.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al. (US 2002/0036536 A1) in view of Iizuka (USP 5585751).

As to claim 2, Wada's figure 2 shows all limitations of the claim except for the variable resistor comprises a plurality of resistive devices in parallel, each of the plurality of resistive devices having a control input node to enable the resistive device. However, Iizuka's figure 3 teaches a variable resistor circuit (8) comprising a plurality of resistive devices (9-13) in parallel,

each of the plurality of resistive devices having a control input node to enable the resistive device (it is inherent for the switches (14-18) having control node for receiving control signals that turn on/off the switches). Therefore, it would have been obvious to one having ordinary skill in the art to use Iizuka's variable resistor for Wada's variable resistor due to doctrine of equivalent functions, and it is seen as an obvious design choice for selecting the digital variable resistor for the Wada's variable resistor.

5. Claims 3-5 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al. (US 2002/0036536 A1) in view of Iizuka (USP 5585751) and Shade, Jr. (USP 4853610).

As to claims 3 and 4, it is inherent for Wada et al.'s figure 2 and Iizuka's figure 3 to have a control circuit to provide control signal(s) to adjust the value of the variable resistor(s). Thus, Wada et al.'s figure 2 shows all limitations of the claim except for the current reference further comprising a control loop circuit to influence the variable resistor. However, Shade, Jr.'s figure 2 shows a method of proving a control signal (output of 27) by using a unity gain amplifier (27) coupled to the output of the control circuit (Po, So, Q1). The unity gain amplifier having the advantage of buffering and providing stronger control signal. Therefore, it would have been obvious to one having ordinary skill in the art to use unity gain amplifier(s) (such as Shade, Jr.'s amplifier 27) as buffer circuit(s) for buffering the control signal(s) that control the impedance of the Wada's variable resistor for the purpose of providing stronger control signal. (The unity gain amplifier having loop structure).

As further called for claim 27, the unity gain amplifier(s) is(are) the variable output driver(s).

As to claim 5, the combination above inherent shows that the control loop (the unity gain amplifier) circuit includes output nodes, and wherein the control input node of each resistive device is coupled to one of the output nodes of the control loop circuit.

Allowable Subject Matter

6. Claims 6 and 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-20 are allowed.

Claims 22-26 are objected.

Claims 6, 28-30 would be allowable because the prior art fails to teach or suggest a circuit (such as figure 3) having a state machine (306) coupled to the output node of the comparator (304), the state machine having output nodes coupled to the control input nodes of the plurality of resistive devices.

Claims 10-20 are allowable because the prior art fails to teach or suggest a circuit (such as figure 3) having a control loop circuit (304, 306) having an input node coupled to an output node of the second current reference, and having an output node to influence the first and second variable resistors.

Claims 21-26 would be allowable because the prior art fails to teach a control loop circuit responsive to a copy of the generated current, the control loop circuit coupled to influence the generated current.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
December 5, 2002

Terry D. Cunningham
Primary Examiner